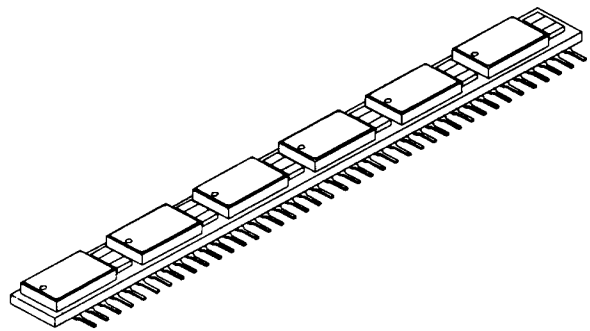
NOT RECOMMENDED FOR NEW DESIGNS

DESCRIPTION:

The DPS384 is a 64K X 6 high-speed, low-power static RAM module comprised of six 64K X 1 monolithic SRAM's, and decoupling capacitors surface mounted on a single inline co-fired ceramic substrate.

The DPS384 operates from a single +5V supply and all input and output pins are completely TTL-compatible. The DPS384 is best suited for high speed military computers and signal processing applications.

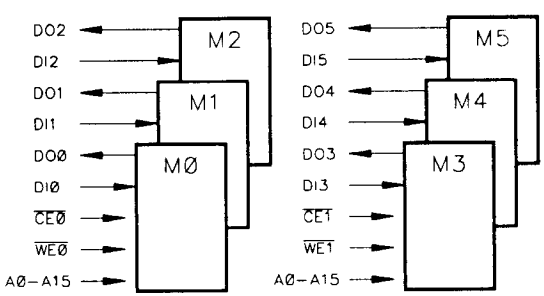


FEATURES:

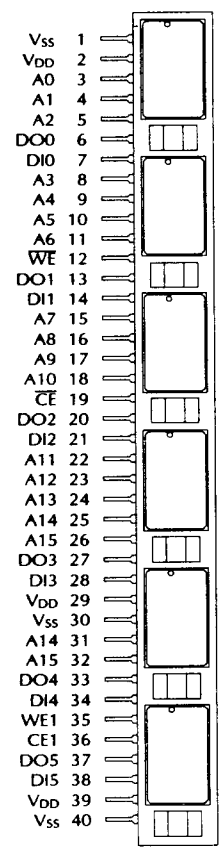
- Organizations Available: 64K X 6 or 128K X 3
- Access Times: 15, 25, 35, 45, 55ns (max.)
- Low Power Dissipation
- Completely Static Operation - No Clock or Refresh Needed
- Three State Output
- All Inputs and Outputs are TTL-Compatible
- 40-Pin SIP

PIN NAMES	
A0 - A15	Address Inputs
DI0 - DI5	Data Inputs
DO0 - DO5	Data Outputs
$\overline{CE0}$ / $\overline{CE1}$	Chip Enables
$\overline{WE0}$ / $\overline{WE1}$	Write Enables
V_{DD}	Power (+5V)
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



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RECOMMENDED OPERATING RANGE [1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.5	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	70	pF	V_{IN} = 0V
C_{CE}	Chip Enable	40		
C_{WE}	Write Enable	40		
$C_{I/O}$	Data Input/Output	25		

ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} + 0.5	V

TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	HIGH-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

H=HIGH L=LOW X=Don't Care

DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	X3		X6		Unit
			Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-60	+60	-60	+60	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	+20	-10	+10	µA
I_{CC1}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, f = 0 Outputs Open		480		630	mA
I_{CC2}	Dynamic Operating Supply Current	Outputs Open $\overline{CE}$ = V_{IL}, f = max.		615		840	mA
I_{SB1}	Standby Supply Current (TTL)	$\overline{CE}$ = V_{IH}		330		330	mA
I_{SB2}	Full Standby Supply Current (CMOS)	$\overline{CE}$ ≥ V_{DD} -0.2V, V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ V_{SS} +0.2V		150		150	mA
V_{OL}	Output Low Voltage	V_{OL} = 8.0mA		0.4		0.4	V
V_{OH}	Output High Voltage	V_{OH} = -4.0mA	2.4		2.4		V

NOTE: Dense-Pac has other specialized suppliers that may provide better A.C. or D.C. Characteristics.

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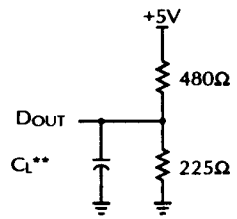
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transient between 0.8V and 2.2V.

Figure 1. Output Load

** Including Probe and Jig Capacitance.



Output Load		
Load	C_L	Parameters Measured
1	30 pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{WLZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{WLZ}

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges [6]

No.	Symbol	Parameter	-15		-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	15		25		35		45		55		ns
2	t_{AA}	Address Access Time		15		25		35		45		55	ns
3	t_{CO}	Chip Enable to Output Valid		15		25		35		45		55	ns
4	t_{OH}	Output Hold for Address Change	5		5		5		5		5		ns
5	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 5]	5		5		5		5		5		ns
6	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 5]		8		15		20		35		35	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

No.	Symbol	Parameter	-15		-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	15		25		35		45		55		ns
11	t_{AW}	Address Valid to End of Write	12		20		30		40		50		ns
12	t_{CW}	Chip Enable to End of Write	12		20		30		40		50		ns
13	t_{DW}	Data Valid to End of Write	14		25		25		25		25		ns
14	t_{DH}	Data Hold Time	0		0		0		0		0		ns
15	t_{WP}	Write Pulse Width	10		15		20		25		35		ns
16	t_{AS}	Address Set-up Time***	5		5		5		5		5		ns
17	t_{AH}	Address Hold Time	5		5		5		5		5		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		15		20		20		25		25	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 5]	5		5		5		5		5		ns

*** Valid for both Read and Write Cycles.

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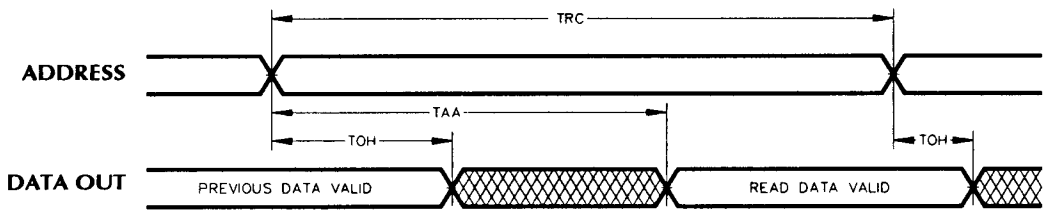
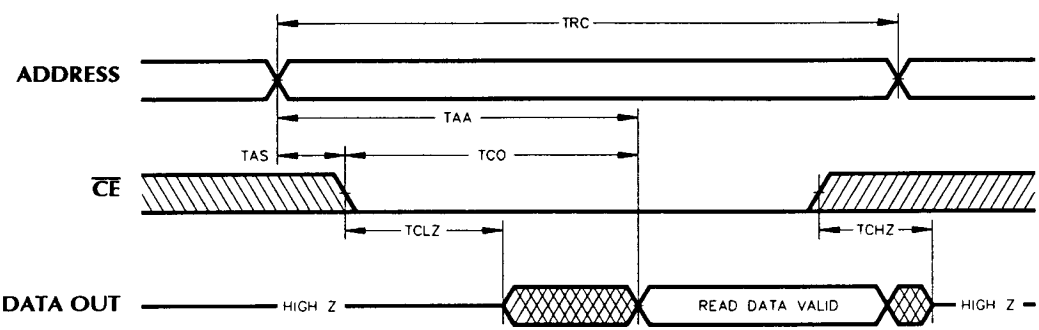
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ is LOW.



READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

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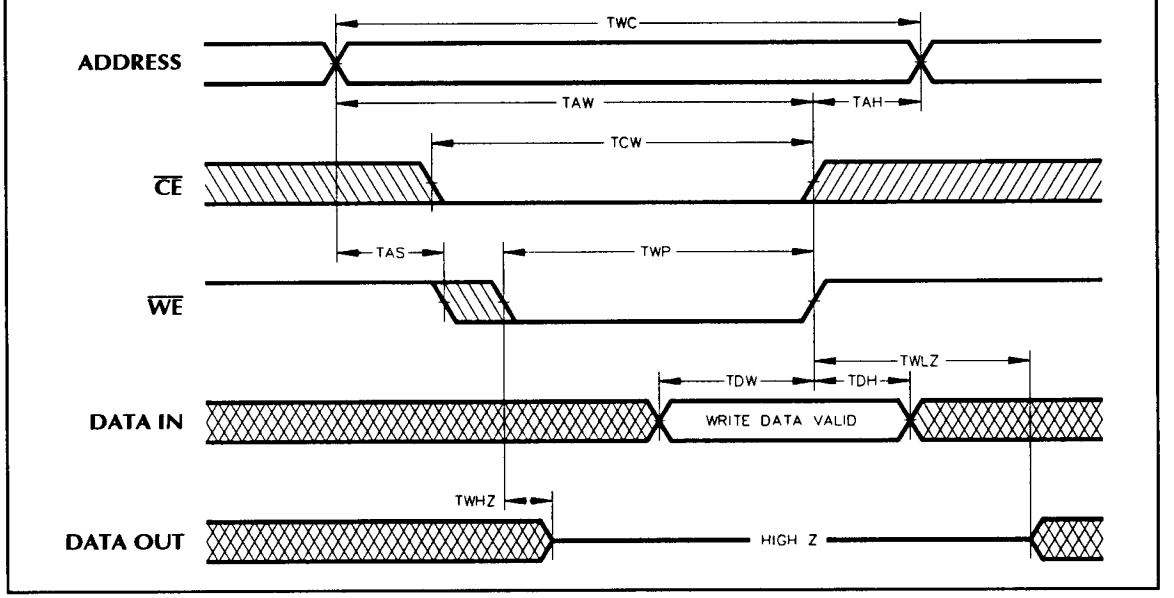
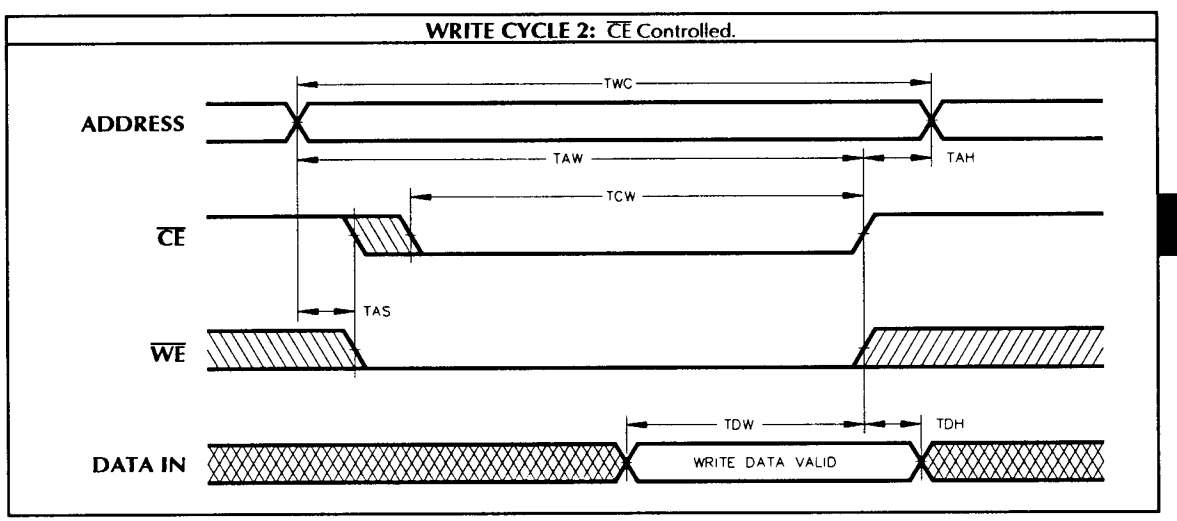
WRITE CYCLE 1: $\overline{WE}$ Controlled.



WRITE CYCLE 2: $\overline{CE}$ Controlled.



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ORDERING INFORMATION

DP S384 – XX X

PREFIX | DEVICE TYPE | SPEED | GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	−40°C to +85°C
M	MILITARY	−55°C to +125°C
B *	MIL−PROCESSED	−55°C to +125°C

15	15ns
25	25ns
35	35ns
45	45ns
55	55ns

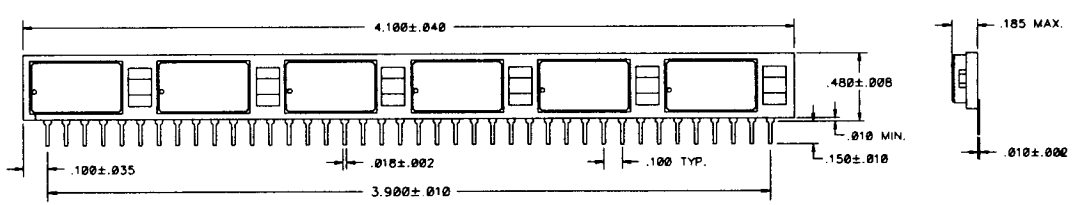
CMOS SRAM 64K X 6 MODULE

* B grade modules built with 883 devices.

NOTES:

1. All voltages are with respect to V_{SS}.
2. -3.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

MECHANICAL DRAWING



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